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10/609,058	06/28/2003	Guangming Yin	BP 2516	6893
34399 7590 04/03/2007 GARLICK HARRISON & MARKISON P.O. BOX 160727 AUSTIN, TX 78716-0727			EXAMINER SINKANTARAKORN, PAWARIS	
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SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/609,058	<b>Applicant(s)</b> YIN ET AL.	
	<b>Examiner</b> Pao Sinkantarakorn	<b>Art Unit</b> 2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 June 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Specification***

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Objections***

2. Claims 1-30 are objected to because of the following informalities:

Regarding claim 1 line 10, the recitation "a transmission time" should be rewritten as ---transmission times---. The same is true for claim 21 line 10.

Regarding claim 7 line 4, the recitation "the at least one second bit" should be rewritten as ---the at least one second bit stream---.

Regarding claim 12 line 2, the recitation "a second data" should be rewritten as --  
-a second bit rate---.

Regarding claim 21 line 10, the recitation "the plurality of symmetrical data pathways" should be rewritten as ---the plurality of symmetrical data circuit pathways---.

The same is true for claim 26 line 10.

Claims 2-11, 13-20, 22-25, and 27-30 are then objected because they depend on claims 1 and 21.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

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The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1- 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 line 16 recites the limitation " the symmetrical pathways ". There is insufficient antecedent basis for this limitation in the claim. It is not known whether the symmetrical pathways are the data circuit pathways or the clock circuit pathways.

Regarding claim 1 line 20, the term "substantially" is vague and indefinite because it is not known the metes and bounds of the claimed invention. This term can be found in many places in the claims.

Regarding claim 12 lines 2, the recitation "the first and second data rate" has no antecedent basis.

Regarding claim 21 line 13, the recitation "the forward data clock signal" has no antecedent basis. The same is true for claim 22 line 3 and claim 27 line 3.

Regarding claim 21 line 15-16, the recitation "the distributed data clock signal" has no antecedent basis. The same is true for claim 26 line 13.

Claims 2-11, 13-20, 23-25, 27-30 are then rejected because they depend on claims 1, 12, 21, and 26.

### ***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 21 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (US 5,940,456).

**Regarding claims 21 and 26**, Chen et al. disclose a multistage bit stream multiplexer/demultiplexer, comprising:

a first multiplexing/demultiplexing integrated circuit that receives a first plurality of bit streams at a first bit rate (see Figure 4 reference numerals 502-505, E1 is the first bit rate) and that produces a second plurality of bit streams at a second bit rate (see Figure 4 reference numerals 502-505, E2 is the second bit rate), wherein the first plurality of bit streams are greater in number than the second plurality of bit streams are in number, and wherein the first bit rate is less than the second bit rate (see Figure 4, E1 is the lowest rate, E2 is the higher rate and E3 is the highest rate);

a clock circuit, wherein the clock circuit generates a forward data clock (see Figure 4 reference numeral 510);

a plurality of symmetrical data circuit pathways that transport the second plurality of bit streams from the first multiplexing/demultiplexing integrated circuit (see Figure 4 "E2 or E3" lines);

a second multiplexing/demultiplexing integrated circuit that receives the second plurality of bit streams from the plurality of symmetrical data pathways (see Figure 4 reference numeral 508, symmetric is interpreted as synchronous), wherein a transmission time for the second plurality of bit streams on the plurality of symmetrical

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data circuit pathways are substantially equal (see column 6 lines 10-15, synchronous multiplexer/demultiplexer synchronizes the second plurality of bit streams) , and wherein the second multiplexing/demultiplexing integrated circuit receives the forward data clock and symmetrically distributes the forward data clock signal along a plurality of symmetrical clock circuit pathways, wherein clock transmission times associated with each clock circuit pathway are substantially equal (see column 6 lines 10-12, synchronous clock synchronizes the transmission times of the clock signals), and wherein the distributed data clock signal latches data from the second plurality of bit streams to produce a high speed bit stream (see Figure 4 "E2 or E3" lines are converted into a high speed line, with E1 being the lowest rate, E2 being the higher rate, and E3 being the highest rate).

***Claim Rejections - 35 USC § 103***

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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8. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 1, 6, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al.

**Regarding claim 1**, Chen et al. disclose a high speed bit stream data conversion circuit (see column 5 lines 58-59, SPDH system) comprising:

a first plurality of input ports that receive a first plurality of bit streams at a first bit rate (see Figure 4 reference numerals 502-505);

a plurality of data conversion circuits that receive the first plurality of bit streams (see Figure 4 reference numerals 502-505) and that produce at least one second bit stream at a second bit rate (see Figure 4 "E2 or E3"), wherein the number and bit rate of the first plurality of bit streams and the at least one second bit stream differ (see Figure 4 the number of "E1 or E2" lines differ from the number of "E2 or E3" lines) ;

a plurality of symmetrical data circuit pathways that comprise pairs of circuit pathways, and that transport the first plurality of bit streams from the first plurality of input ports, and to the plurality of data conversion circuits, wherein transmission times for the first plurality of bit streams on the plurality of symmetrical data circuit pathways are substantially equal (see Figure 4 "E1 or E2" lines coupled to reference numerals 502-505, the lines are of the same length; therefore, transmission times should be substantially equal);

a clock distribution circuit that receives a data clock signal at a clock port (see Figure 4 reference numeral 510), and symmetrically distributes the data clock signal to the plurality of data conversion circuits along a plurality of symmetrical clock circuit pathways (see Figure 4 reference 510 and column 6 lines 10-12, symmetrically is interpreted as synchronously), wherein the pathways further comprise a central trunk coupled to the clock port and wherein the trunk is located between a first pair of circuit pathways, and symmetrical pairs of branches that extend from the trunk and couple to the data conversion circuits (see Figure 4 clock line coupled to reference numerals 510 and 502-505), and wherein the clock transmission times associated with each clock circuit pathway are substantially equal (see Figure 4 reference numeral 510, synchronous clock synchronizes clock signals transmitted to data conversion circuits), and wherein the distributed data clock signal latches data in the data conversion circuits from the first plurality of bit streams to the second plurality of bit streams (see Figure 4 "E1 or E2" lines are converted into "E2 or E3" lines, with E1 being the lowest rate and E3 being the highest rate), and wherein the pairs of circuit pathways comprise a first



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pathway located on a first side of the trunk and a second pathway located on a second side of the trunk, wherein the second side is opposite the first side (see Figure 4 reference numeral 510, synchronous clock receives a clock signal from a signal source, which is not shown, and distributes synchronous clock signals to data conversion circuits 502-505 and 510).

Chen et al. disclose all the subject matter of the claimed invention except the clock being located at a midpoint of the first plurality of input ports. However, it is well known in the art to locate the clock at a midpoint of the first plurality of input ports.

Thus, it would have been obvious to the person of ordinary skill in the art to locate a clock at a midpoint of the first plurality of input ports in the data conversion circuits of Chen et al.

The motivation for locating the clock at a midpoint of the first plurality of input ports is that it reduces the cost of wiring and it provides a better layout of the circuits.

Claim 12 is rejected for the same reason as claim 1, since claim 12 is a method for performing the apparatus of claim 1.

**Regarding claim 6**, wherein the plurality of symmetrical data circuit pathways that transport the first plurality of bit streams are symmetrical with respect to the symmetrical clock circuit pathways (see Figure 4, reference numerals 502-503 are symmetrical with 504-505 about reference numeral 508).

**Regarding claim 11**, Chen et al. disclose all the subject matter of the claimed invention except the conversion circuit, wherein a physical length of each symmetrical data circuit pathways is substantially equal, and wherein a physical length of each

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symmetrical clock circuit pathways is substantially equal. However, it is well known in the art to implement the pathways of the same length.

Thus, it would have been obvious to the person of ordinary skill in the art to implement pathways of the same length in the data conversion circuits of Chen et al.

The motivation for implementing pathways of the same length is that it provides easier implementation of the circuit.

11. Claims 2, 7-10, 13, 22, 25, 27, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Dorschky (US 6,636,532).

**Regarding claims 2, 7, 22, 25, 27, and 30**, Chen et al. disclose all the subject matter of the claimed invention except the retimer that ensures data integrity between the first plurality of bit streams and the at least one second bit stream, and the plurality of delay elements operable to compensate for skewing of the data clock signal received by each data conversion circuit.

The invention of Dorschky from the same or similar fields of endeavor disclose a plurality of delay elements operable to compensate for skewing of the data clock signal received by each data conversion circuit (see Figure 1 T1-Tm and column 2 lines 1-29, the multiplexing of data signals by each multiplexer is clocked by the common clock signal via the delay lines T1-Tm; the delayed clock signals are used as a retimer to clock each multiplexer).

Thus, it would have been obvious to the person of ordinary skill in the art to implement delay elements of Dorschky into the data conversion circuits of Chen et al.

The motivation for implementing delay elements into the data conversion circuits is that it provides a more efficient data conversion circuit.

Claim 13 is rejected for the same reason as claim 2, since claim 13 is a method for performing the apparatus of claim 2.

**Regarding claim 8**, Chen et al. disclose the data conversion circuit comprises a multiplexer, wherein a number of first bit streams exceeds a number of second bit streams, and wherein the second bit rate exceeds the first bit rate (see Figure 4 reference numerals 502-505, E1 is the lowest rate and E3 is the highest rate).

**Regarding claims 9 and 10**, Chen et al. disclose all the subject matter of the claimed invention except the plurality of first bit streams comprise 4 or 16 bit streams at a bit rate of about 10 or 2.5 Gbps, and wherein the at least one second bit stream comprises 1 bit stream at a bit rate of about 40 or 10 Gbps. However, it is well known in the art to generate signals of bit rate as low as 2.5 Gbps and to implement a conversion circuit that is capable of converting a low bit rate into a bit rate as high as 40 Gbps.

Thus, it would have been obvious to the person of ordinary skill in the art to generate signals of bit rate as low as 2.5 Gbps and to implement a conversion circuit that is capable of converting a low bit rate into a bit rate as high as 40 Gbps in the data conversion circuits of Chen et al.

The motivation for generating signals of bit rate as low as 2.5 Gbps and implementing a conversion circuit that is capable of converting a low bit rate into a bit rate as high as 40 Gbps is that it provides a faster data transmission.

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12. Claims 3-5, 14-20, 23, 24, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Dorschky as applied to claims 2 and 13 above, and further in view of Okayasu (US 2001/0005158).

**Regarding claims 3-5, 23, 24, 28, and 29,** Chen et al. in view of Dorschky disclose all the subject matter of the claimed invention except the switched capacitor networks that introduce delay increments based on a capacitance coupled to a buffer amplifier.

The invention of Okayasu from the same or similar fields of endeavor disclose a variable delay circuit operable to delay a clock signal with variable capacitance (see paragraph 88, the voltage/load capacity-control-type variable delay element delays a referential clock by the M number of the voltage/load capacity-control-type variable delay elements)

Thus, it would have been obvious to the person of ordinary skill in the art to implement a voltage/load capacity-control-type variable delay element as taught by Okayasu into the data conversion circuits of Chen et al.

The motivation for implementing the voltage/load capacity-control-type variable delay element is that it provides a more efficient data conversion circuit by adjusting the capacitor value in the voltage/load capacity-control-type variable delay element to generate a desired delay amount.

Claims 14-16 are rejected for the same reason as claims 3-5, since claims 14-16 are methods for performing the apparatus of claims 3-5.

**Regarding claim 17**, Chen et al. disclose the data conversion circuit comprises a multiplexer, wherein a number of first bit streams exceeds a number of second bit streams, and wherein the second bit rate exceeds the first bit rate (see Figure 4 reference numerals 502-505, E1 is the lowest rate and E3 is the highest rate).

**Regarding claims 18 and 19**, Chen et al. disclose all the subject matter of the claimed invention except the plurality of first bit streams comprise 4 or 16 bit streams at a bit rate of about 10 or 2.5 Gbps, and wherein the at least one second bit stream comprises 1 bit stream at a bit rate of about 40 or 10 Gbps. However, it is well known in the art to generate signals of bit rate as low as 2.5 Gbps and to implement a conversion circuit that is capable of converting a low bit rate into a bit rate as high as 40 Gbps.

Thus, it would have been obvious to the person of ordinary skill in the art to generate signals of bit rate as low as 2.5 Gbps and to implement a conversion circuit that is capable of converting a low bit rate into a bit rate as high as 40 Gbps in the data conversion circuits of Chen et al.

The motivation for generating signals of bit rate as low as 2.5 Gbps and implementing a conversion circuit that is capable of converting a low bit rate into a bit rate as high as 40 Gbps is that it provides a faster data transmission.

**Regarding claim 20**, Chen et al. disclose all the subject matter of the claimed invention except the conversion circuit, wherein a physical length of each symmetrical data circuit pathways is substantially equal, and wherein a physical length of each symmetrical clock circuit pathways is substantially equal. However, it is well known in the art to implement the pathways of the same length.

Thus, it would have been obvious to the person of ordinary skill in the art to implement pathways of the same length in the data conversion circuits of Chen et al.

The motivation for implementing pathways of the same length is that it provides easier implementation of the circuit.

### ***Conclusion***

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mori et al. (US 4,727,541), Shimada et al. (US 5,726,990), and Karlquist (US 2003/0063626) are cited to show systems/methods that are considered pertinent to the claimed invention.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pao Sinkantarakorn whose telephone number is 571-270-1424. The examiner can normally be reached on Monday-Thursday 9:00am-3:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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PS



RICKY Q. NGO  
SUPERVISORY PATENT EXAMINER